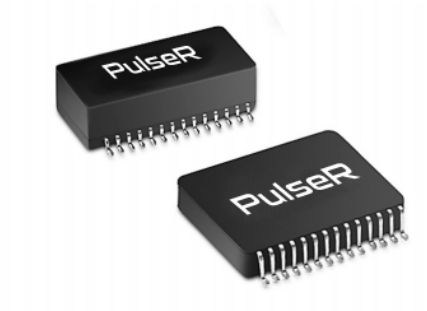
COPPERHEAD SERIES FIBRE CHANNEL TRANSCEIVER

Line Interface Module

Ruggedized



- High Performance, low cost alternative to completely fiber systems
- Compact small Package saves PCB foot print Equalizer and transformers isolation provides long distance applications , better transient protection and common mode rejection.
- Low transmit/receive jitter
- Low Power dissipation; 300mW typical
- Operating Temperature -55°C to +125°C
- Moisture Sensitivity Level: 3

Transmitter		Vcc = 3.15V to 3.45V			
Parameter	SYM	MIN	Typical	MAX	UNIT
Input Data Voltage Low	VIL	1.35	—	1.88	V
Input Data Voltage High	VIH	2.07	—	2.58	—
Differential Input Data Voltage	VIN	150	800	1200	mV P-P
Input High Voltage	—	—	—	—	—
Common Mode Range(Differential)	VIHCMR	2	—	3.3	V
Transmitte Output Impadence (Diff)	Ztx-Diff	100	150	—	Ohma
Output Differential signal level (p-p)	VOT	1100	1250	—	mV
Data Rate (NRZ)	DR	—	1062	—	Mb/s
Total P-P transmit jitter (Dj=Rj)	TPK-PK	—	180	235	ps
Output rise-fall time (20%-80%)	TRO	—	—	430	ps

Receiver		Vcc = 3.15V to 3.45V			
Parameter	SYM	MIN	Typical	MAX	UNIT
Input Voltage swing(Differential)	VIN-P-P	150	—	1200	mV
Differential Output Data Voltage	VO-Diff.	500	—	1000	mV
OutputCommon-Mode Voltage	VO-comm	1.75	1.93	2.05	V
Data Rate (NRZ)	DR	—	1062	—	Mb/s
Total P-P transmit jitter (Dj=Rj)	TPK-PK	—	375	526	ps
Return Loss, Input	S11	-15	-17	—	dB

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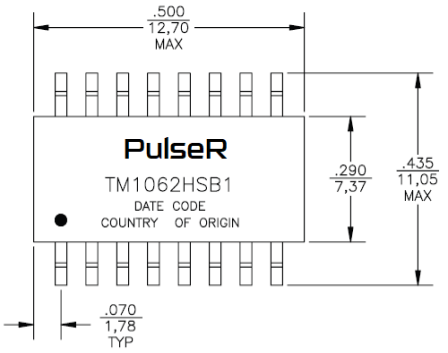
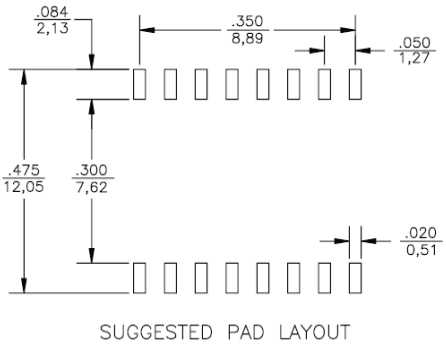
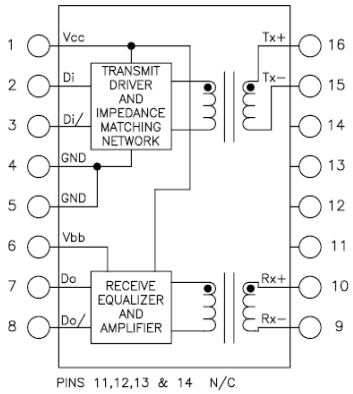
Mechanical

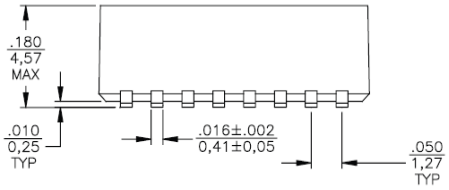
Schematic

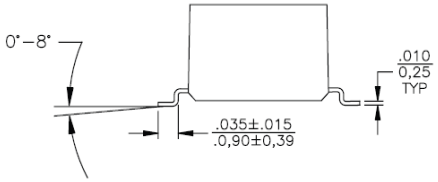
TM1062HSB1









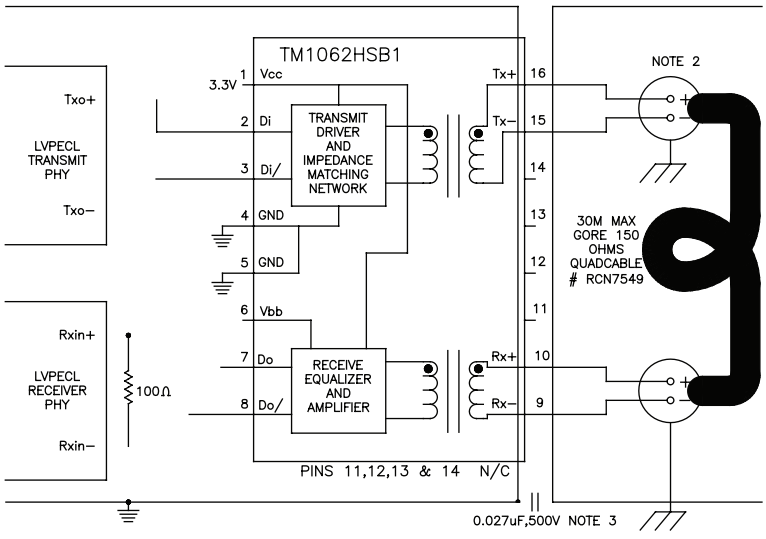


WEIGHT.....1.0 grams
Tape & Reel.....400/reel

Dimensions: Inches / mm

Unless otherwise specified, all tolerances are ±.005 / 0.13

Suggested Application For LVPECL Interface

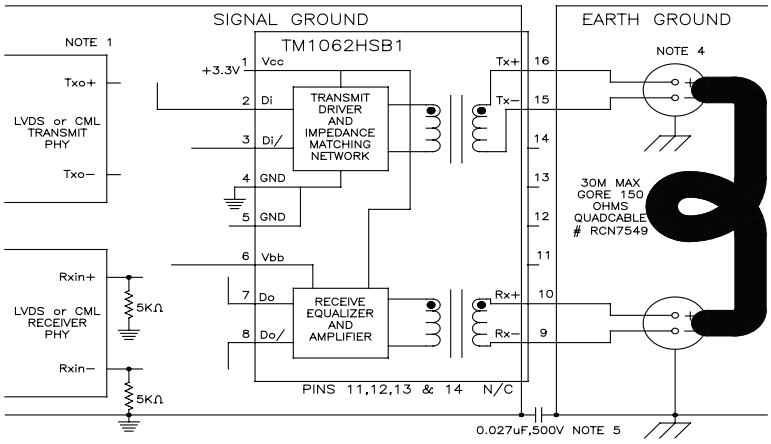


NOTE 1.
WHEN LAYING OUT PCB CABLE SIDE SIGNAL LINES SHALL BE 150 OHMS DIFFERENTIAL–CONTROL IMPEDANCE MICRO STRIP LINE TRACES AND PHY SIDE SIGNAL SHALL BE 100 OHMS DIFFERENTIAL CONROL IMPEDANCE MICRO STRIP LINE TRACES.

NOTE 2.
CABLE CONNECTOR SHALL BE PLACED AS CLOSE AS POSSIBLE TO PULSE FIBER CHANNEL TRANSCIEVER.

NOTE 5.
IT IS RECOMMENDED THAT SIGNAL GROUND FOR PHY SIDE AND CHASSIS GROUND FOR CABLE SIDE SHALL BE SEPERATE GROUND CABLE SHIELD BE CONNECTED TO CHASSIS GROUND. BOTH GROUNDS SHOULD BE AC COUPLED WITH 0.027uF, 500V CAPACITOR.

Suggested Application For LVDS and CML Interface



NOTE 1.
FOR LVDS AND CML TRANSMIT INTERFACE AC COUPLE Di & Di/ LINE WITH 0.1 uF HI QUALITY CHIP CAPACITOR AND TERMINATE Di & Di/ (PINS 2 & 3) IN TO 50 OHMS TO Vbb (PIN 6) AS SHOWN ABOVE.

NOTE 2.
FOR LVDS AND CML RECEIVE INTERFACE AC COUPLE Do & Do/ LINE WITH 0.1 uF HI QUALITY CHIP CAPACITOR AND TERMINALTE Do & Do/ LINE AT LVDS RECEIVER INPUT PINS IN TO 5.0K OHMS TO GROUND TO BIAS THE COMMON−MODE VOLTAGE. CML RECEIVER DOES NOT REQUIRED ANY TERMINATION AS EACH INPUT HAS INTERVAL 50 OHMS TO Vcc TERMINATION (5K OHMS TERMINATION IS NOT REQUIRED FOR CML PHY).

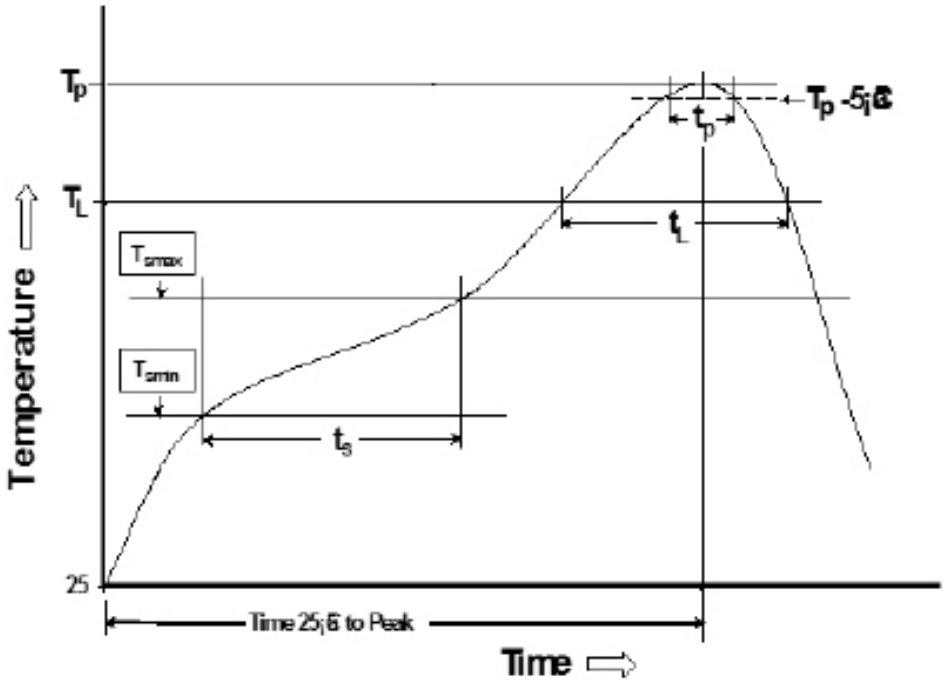
NOTE 3.
WHEN LAYING OUT PCB CABLE SIDE SIGNAL LINES SHALL BE 150 OHMS DIFFERENTIAL−CONTROL IMPEDANCE MICRO STRIP LINE TRACES AND PHY SIDE SIGNAL SHALL BE 100 OHMS DIFFERENTIAL CONROL IMPEDANCE MICRO STRIP LINE TRACES.

NOTE 4.
CABLE CONNECTOR SHALL BE PLACED AS CLOSE AS POSSIBLE TO PULSE FIBER CHANNEL TRANSCIEVER.

NOTE 5.
IT IS RECOMMENDED THAT SIGNAL GROUND FOR PHY SIDE AND CHASSIS GROUND FOR CABLE SIDE SHALL BE SEPERATE GROUND CABLE SHIELD BE CONNECTED TO CHASSIS GROUND. BOTH GROUNDS SHOULD BE AC COUPLED WITH 0.027uF, 500V CAPACITOR.

Pin number(s)	
1…….…...	The positive supply for the line interface module. Connect to +3.3V for PECL application.
2, 3 …….…...	Di, Di/ : Differential PECL compatible data inputs to the transmitter side of the module. Di, Di/ should be control impedance 100 ohm differential line. If input to Di, Di/ is not PECL compatible Di/, Di should AC coupled with 0.1 uF close to pin 1 and 2 .and biased up to PECL common mode +2.0 V dc using 50 Ω to pin 1 and pin 2 (100 Ω differential).
4,5…….	Signal Gnd: The negative supply for the line interface module. Connect to Gnd for PECL applications.
6 …….....	Vbb : Output ,PECL common mode voltage reference.
7,8 …….....	DO , DO/ : Differential PECL data outputs. Terminate both output with 150 Ω to ground. Traces should be control impedance 100 ohm differential , can be terminated 100 ohms diff. at the receiver chip. If receiver is not PECL input Do and Do/ should be AC coupled with 0.1 uF close to pin 2 and 3 into 100 ohm differential line .Far end(at receiver chip) Do, Do/ should be terminated with 50 ohms to bias voltage Vbb. (this will terminate differential line into 100 ohm.)
9,10 …….…...	R X -, R X + : Transformer coupled differential inputs to receiver section Internally terminated for 150 Ω cable. For single ended coax applications, R X -should be connected to shield of cable/earth Gnd; R X + should be connected to the center conductor. Earth Gnd should be AC coupled to DC signal Gnd using a 0.027 µF capacitor, ~500V.
11,12,13,14….	No internal connection to these pins.
15, 16 …….…...	T X - , T X + : Transformer coupled differential outputs to 150Ω cable. For coax applications Tx-,should be connected to shield of cable/earth Gnd; T X + should be connected to the center conductor. Earth Gnd should be AC coupled to DC signal Gnd using a 0.027 µF capacitor, 500V.

Tin/Lead Recommended Reflow Profile (Based on J-STD-020D)



T_{SMIN} (°C)	T_{SMAX} (°C)	T_L (°C)	T_P (°C MAX)	t_S (s)	t_L (s)	t_P (s MAX)	Ramp-up rate (T_L to T_P)	Ramp-down rate (T_P to T_L)	Time 25°C to peak temperature (s MAX)
100	150	183	235	60-120	60-150	20	3°C/s MAX	6°C/s MAX	360

Notes:

1. All temperatures measured on the package leads.
2. Maximum times of reflow cycle: 2.

For More Information
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